

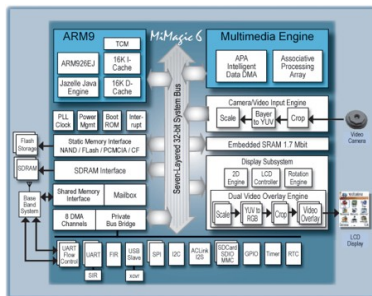
Contract Based Coordination of Hardware Components for the Development of Embedded Software

Tayeb Bouhadiba & Florence Maraninchi



09-12 June 2009

Embedded Software For Systems-on-a-Chip

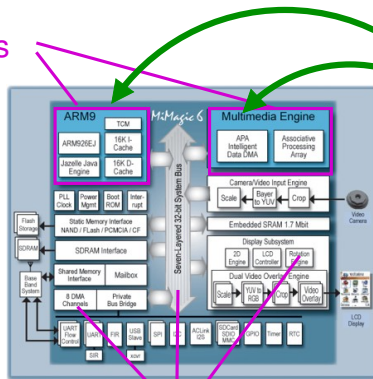


Hardware



Embedded Software For Systems-on-a-Chip

Processors



Software

+

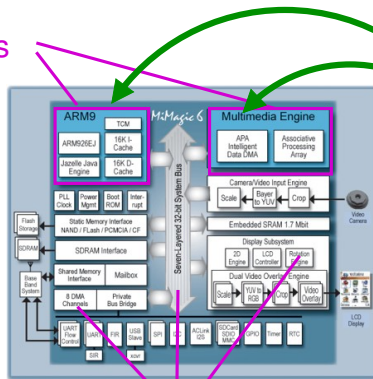
Hardware

Hardware IP's
(components)



Embedded Software For Systems-on-a-Chip

Processors



Software

+

Hardware
(Dedicated)

Hardware IP's
(components)

⇒ Need for Virtual Prototypes of the Hardware
(Virtual Prototypes == Executable Models)



Executable HW Models for SW Development

- RTL (Register Transfer Level) Model
 - Accurate, Late availability, Low co-simulation speed



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- High Level Models
 - Early available, Fast simulation, Abstract



Executable HW Models for SW Development

- RTL (Register Transfer Level) Model
 - Accurate, Late availability, Low co-simulation speed
 - need to speed up simulation

- High Level Models
 - Early available, Fast simulation, Abstract
 - SystemC-TLM is a standard in the industry (TLM: Transaction Level Modeling)



Motivation of the work

- Component-based Virtual Prototyping of Hardware
- As Abstract As Possible
- Software Execution on the Simulated Hardware
- Inspired From SystemC-TLM but Formal and Language-Independent (Using the 42 Component Model [GPCE'07])

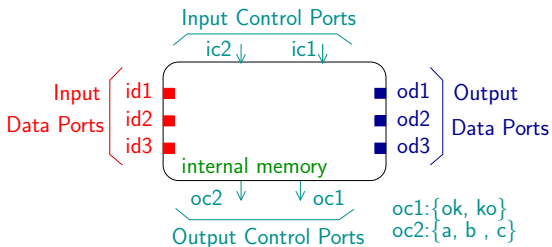


Content

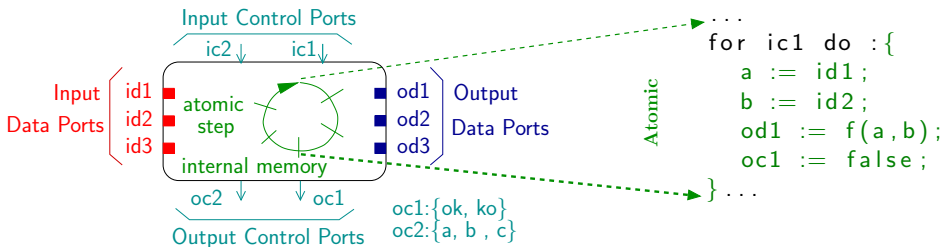
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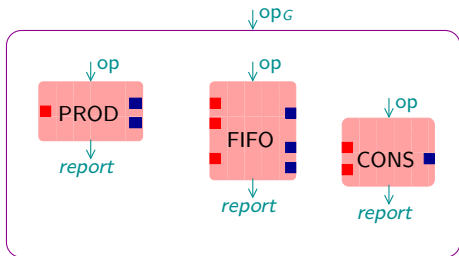
42 in a Nutshell: Basic Components



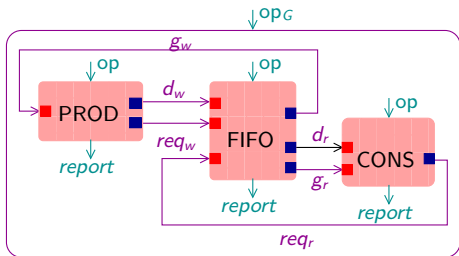
42 in a Nutshell: Basic Components



42 in a Nutshell: Assembling Components

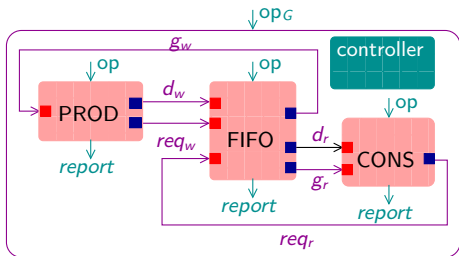


42 in a Nutshell: Assembling Components



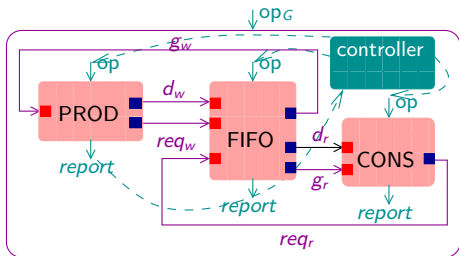
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For each OP_G the controller:



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For each OP_G the controller:
 Activates PROD, CONS, FIFO through op
 Reads their output control ports (report)



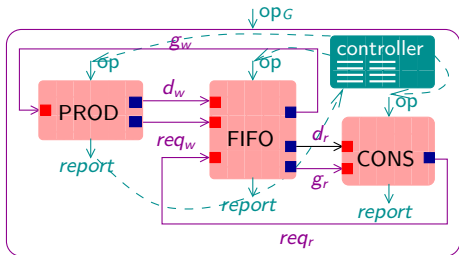
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For each OP_G the controller:

Activates PROD, CONS, FIFO through op

Reads their output control ports (report)

Manages a temporary memory (req_r , dr , req_w , $dw...$)



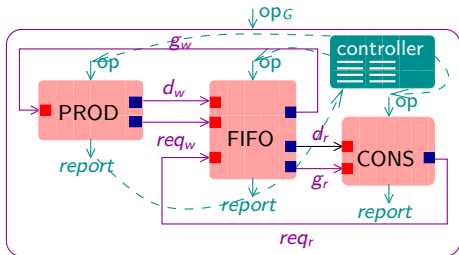
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42 in a Nutshell: Assembling Components

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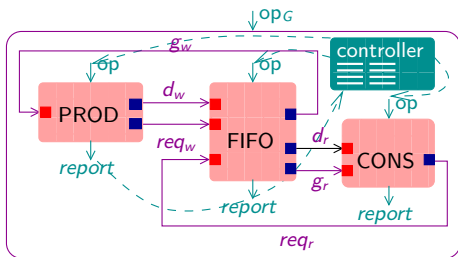
Controller is {
  var M : bool;
  for OPG do { /* defines opg.
    dw, dr, reqw, ...: fifo(1,int);
    M := random();
    if (M) {
      PROD.op ; reqw.put; reqw.get;
      FIFO.op ; gw.put; gw.get;
      a := FIFO.report; /* reads
      if(a==ok){ output control
        PROD.op;dw.put; dw.get;
        FIFO.op; /* activate FIFO
        ...
      }
      ...
    }else{
      CONS.op; reqr.put; reqr.get;
      FIFO.op ; gr.put; gr.get;
      a := FIFO.report;
      ...
    }
  }
}

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For each OP_G the controller:

Activates PROD, CONS, FIFO through op
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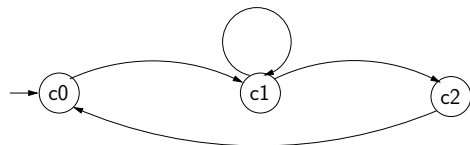
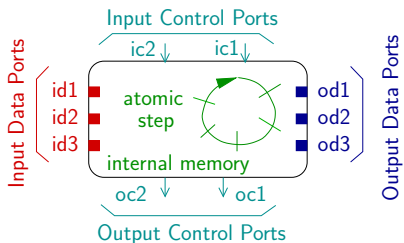


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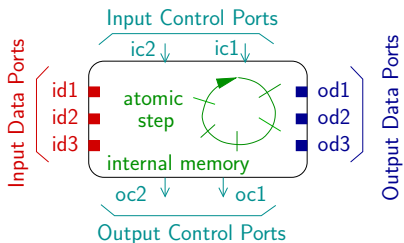
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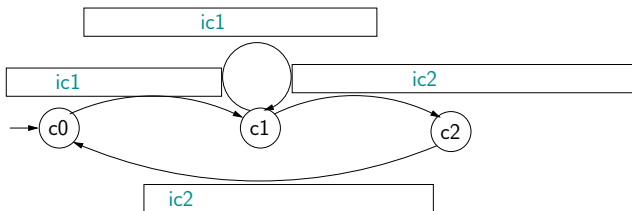
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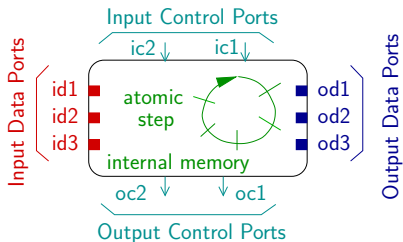
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- Allowed activation sequences
 - It recognizes the correct sequence of activations since the first activation
 - Each state is an accepting state

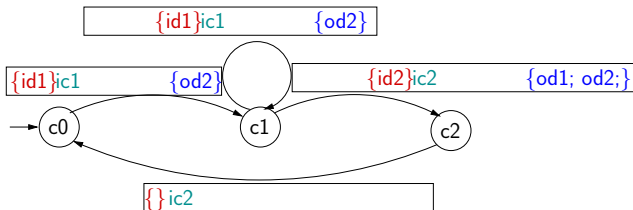


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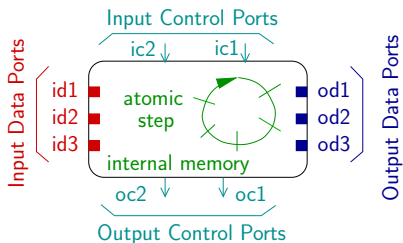


Output Data Ports

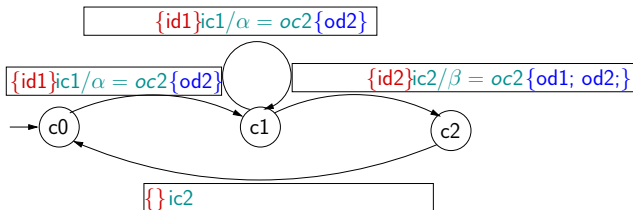
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- Data dependencies (**Required**, **Provided**)
 - Don't care about values except for particular data ports



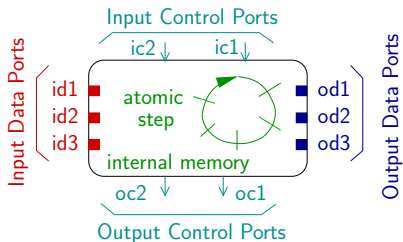
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- Control information

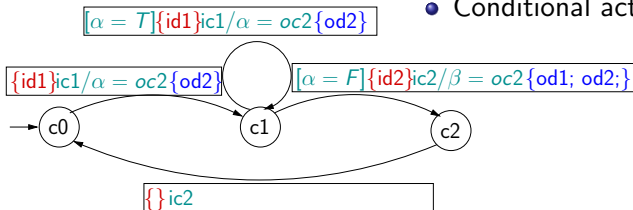


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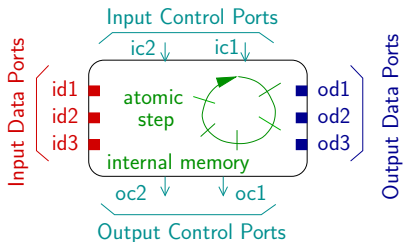


Output Data Ports

- Allowed activation sequences
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- Conditional activations.

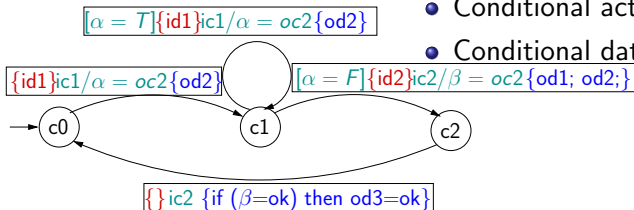


Control Contracts for 42 Components

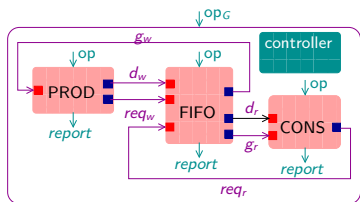


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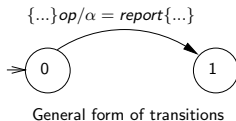
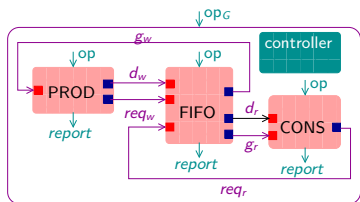
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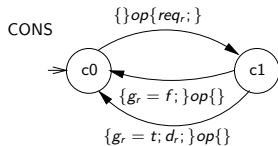
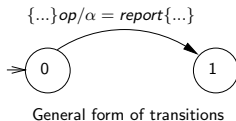
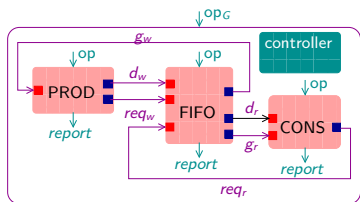
42 Contracts: Example



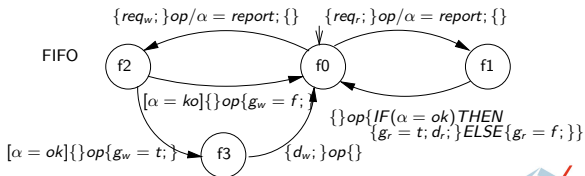
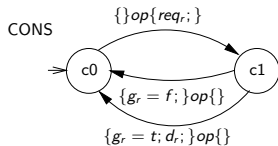
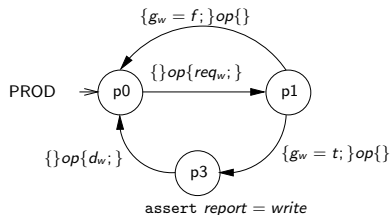
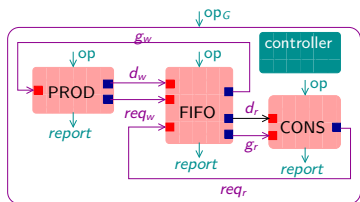
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Controllers as Contracts Interpreters

The controller maintains:

p_0, f_0, c_0

- The current state of each contract



Controllers as Contracts Interpreters

The controller maintains:

- The current state of each contract
- The set of available data

$$p0, f0, c0$$
$$available = \{ \}$$


Controllers as Contracts Interpreters

The controller maintains:

- The current state of each contract
- The set of available data
- The values of the variables(α)

$$\begin{array}{l} p0, f0, c0 \\ \text{available} = \{ \} \\ \alpha = \text{null} \end{array}$$



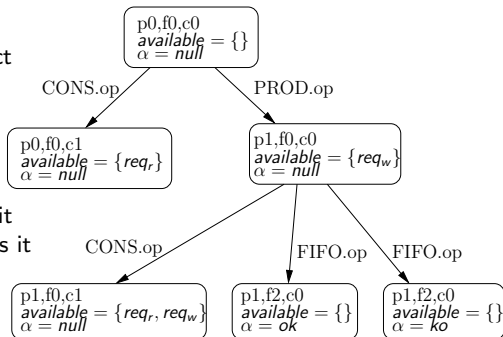
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For each global activation :

- Depending on the available data it selects a component and activates it
- The output controls are given non-deterministic values
- The set of available data is updated



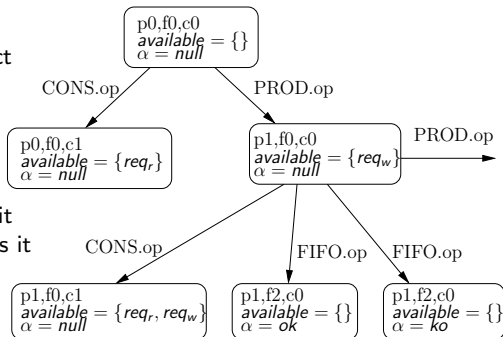
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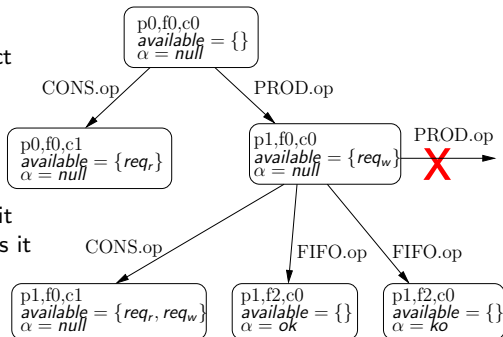
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Summary

- Contracts are non-deterministic abstractions of the components' behaviors and allow for early execution
- Contracts interpreters expose the possible interleavings of the components' behaviors



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Modeling Hardware with 42: Case Study

Embedded Software

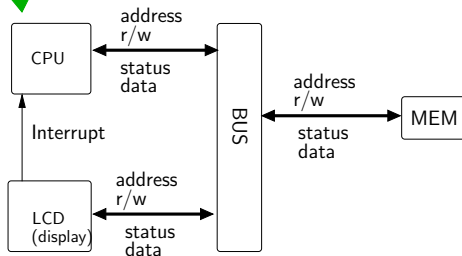
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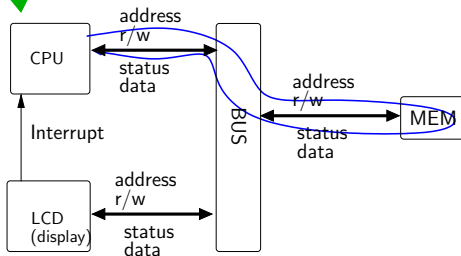
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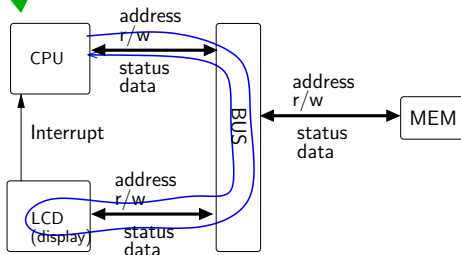
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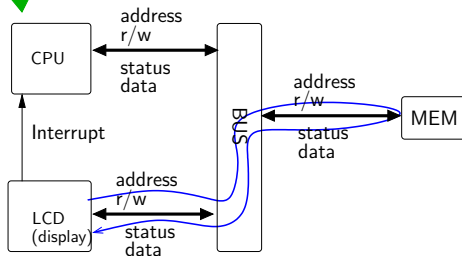
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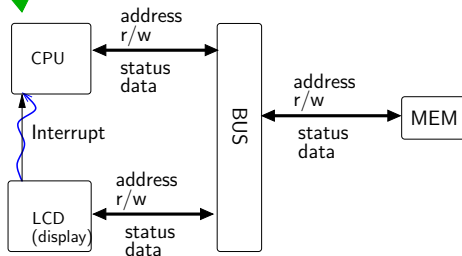
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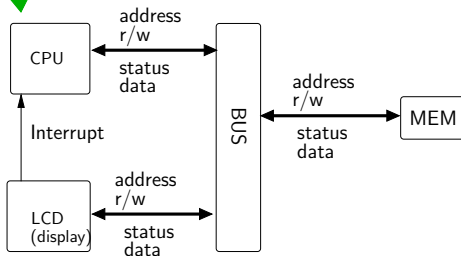
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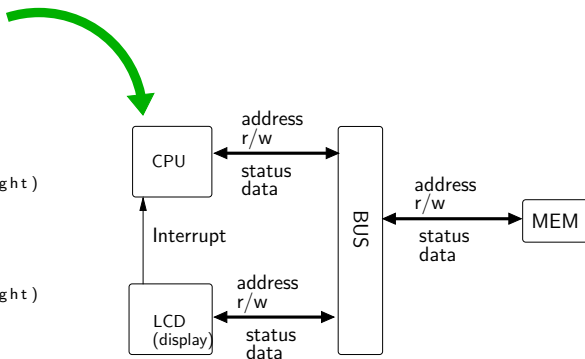
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a
ok



b



c



d



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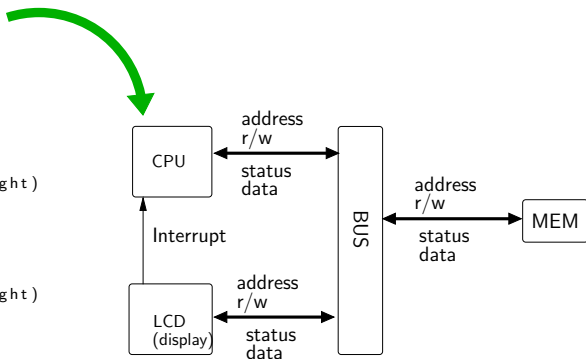
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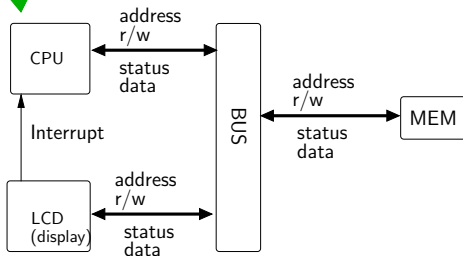
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  write_lcd(0x01,0x1);
  wait_interrupt ();

  /*writing the red image*/
  for(int x=0; x<width * height)
    write_mem(red);
  write_lcd(0x01,0x1);
  wait_interrupt ();
}
}

```



a
ok



b
ok



c
bug
(Synchronization)



d



Modeling Hardware with 42: Case Study

Embedded Software

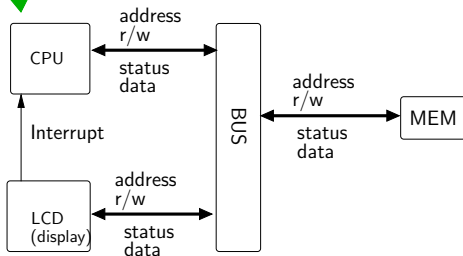
```

#define width 240
#define height 240
#define green 0x0000AABB
...
int main() {
while(1) {
  /*writing the green image*/
  for(int x=0; x<width * height)
    write_mem(green);
  write_lcd(0x01,0x1) ;
  wait_interrupt();

  /*writing the blue image*/
  for(int x=0; x<width * height)
    write_mem(blue);
  write_lcd(0x01,0x1);
  wait_interrupt();

  /*writing the red image*/
  for(int x=0; x<width * height)
    write_mem(red);
  write_lcd(0x01,0x1);
  wait_interrupt();
}
}

```



a
ok



b
ok



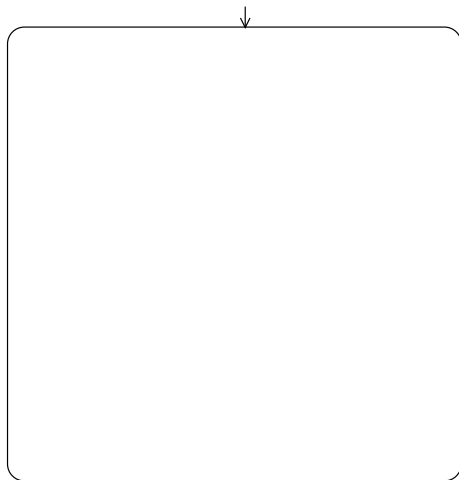
c
bug
(Synchronization)



d
bug
(Data)



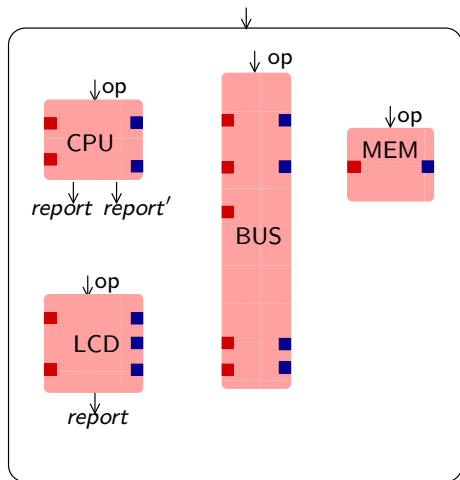
Modeling Hardware with 42: The 42 Model



- The Chip is modeled as a 42 component



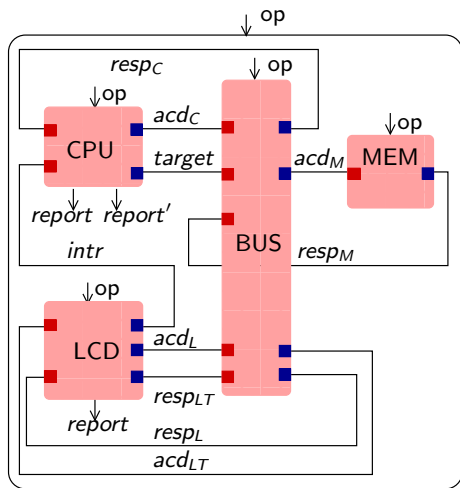
Modeling Hardware with 42: The 42 Model



- The Chip is modeled as a 42 component
- Each HW component too



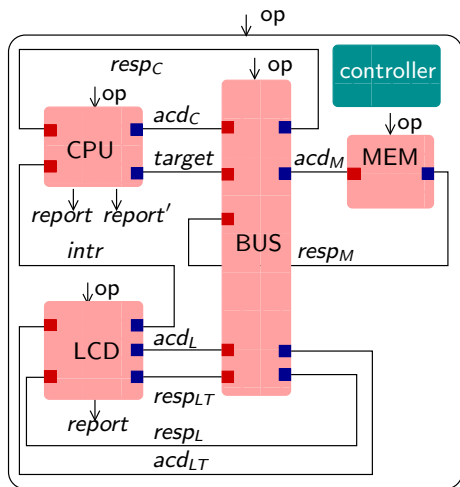
Modeling Hardware with 42: The 42 Model



- The Chip is modeled as a 42 component
- Each HW component too
- Connections correspond to HW communication wires



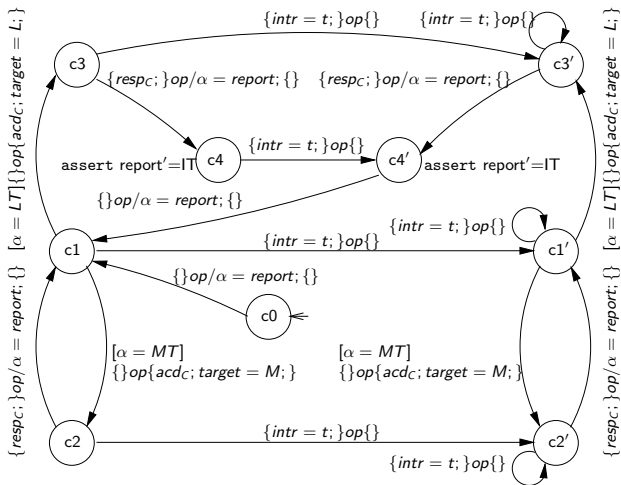
Modeling Hardware with 42: The 42 Model



- The Chip is modeled as a 42 component
- Each HW component too
- Connections correspond to HW communication wires
- The controller is a contract interpreter



Modeling Hardware with 42: The contracts (CPU)



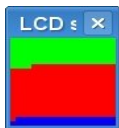
The contract of the CPU is in fact the contract of (CPU + Software)



Detecting Synchronization Bugs by Executing contracts

We don't have the software yet. We execute only the contracts.

- **Example Bug:** The software doesn't wait for interrupts
- **Consequence:**



- **Detection:** Deadlock during contracts interpretation



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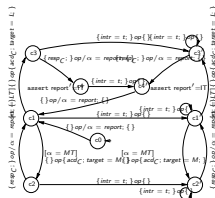
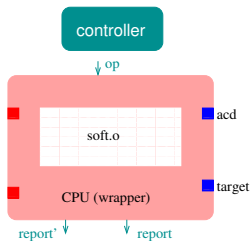
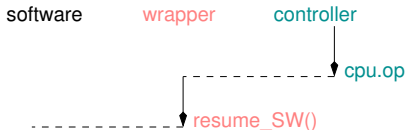


Executing the Real Software on HW Models

```

➔ a) int main(){
    while (true){
        int x = ....
        while(x>0){
            x - -;
            ...
        }
        b) write_mem(adr, data);
        ...
        ...
        d) write_lcd(adr2, data2);
        if(y!=0)
        e) write_mem(adr, data)
        ...
    }
}

```

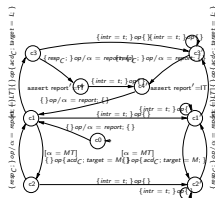
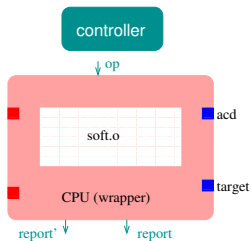
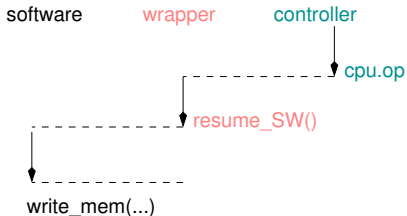


Executing the Real Software on HW Models

```

atomic
  a) int main(){
      while (true){
        int x = ....
        while(x>0){
          x - -;
          ...
        }
        b) write_mem(adr, data);
        ...
        ...
        d) write_lcd(adr2, data2);
        if(y!=0)
        e) write_mem(adr, data)
        ...
      }
  }

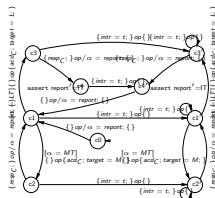
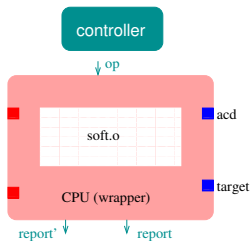
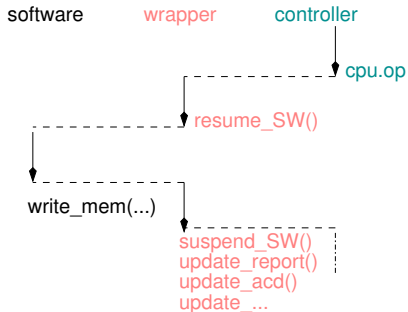
```



Executing the Real Software on HW Models

```

atomic
  a) int main(){
      while (true){
        int x = ....
        while(x>0){
          x - -;
          ...
        }
        b) write_mem(adr, data);
        ...
        d) write_lcd(adr2, data2);
        if(y!=0)
        e) write_mem(adr, data)
        ...
      }
  }
  
```



Detecting Data Bugs

The real software is executed with the contracts together with the rest of the components' implementations.

- **Example bug:** Display dimensions are not correct
- **Consequence:**



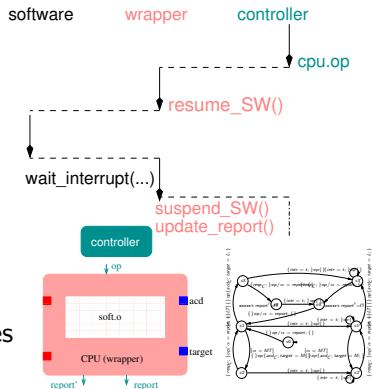
- **Detection:** Visualizations



Compatibility of the Software with the Contracts

We use the contracts as monitors, the wrapper reports on the activity of the software through control output.

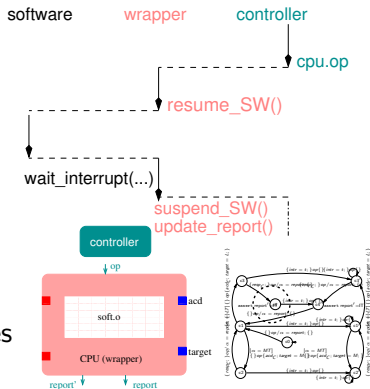
- **Example bug:** The software doesn't call `wait_interrupt()` when expected
- **Consequence:** An unexpected value of output control values
- **Detection:** Assertions on output control ports values associated with contracts states



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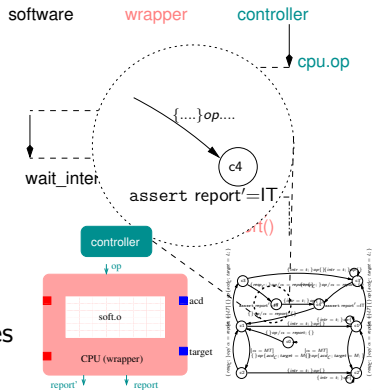
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Conclusion

We defined executable contracts for the modeling of hardware components. It is SystemC-TLM like approach but formal and language-independent.

Typical uses of the approach:

- Modeling the architecture with 42 components
- Executing the contracts alone to detect synchronization bugs
- Implementing the software
- Executing SW+contracts to check compatibility
- Debug and detect data-related bugs



Perspectives

- Adapting the approach to the SystemC-TLM (Submitted to EmSoft09)
- Mixing 42 Contracts and SystemC components
- Extensions to hierarchical contracts interpreters



Questions?

